

# Power Factor Correction Circuit and Output Analysis Based on Rejection Harmonies

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**Abstract**— The aim of the project is to develop a buck-boost converter that improves the input power factor of AC power supplied by activating the AC input current waveform. The main functionality of the project is to provide a near unity power factor for the buck-boost operation and reduce the total harmonic distortion. Due to increase in the use of converters in industries and home, low power factor conversion results in huge losses of power. To fill this gap, a near unity power factor is designed for the buck boost operation. The project will solve the problems of manual monitoring and provides a platform to perform actions without the presence of user near the hydroponics system. For PFC BBC, the suggested control methodology utilizes a Proportional-Integral (PI) controller in the outer voltage loop and an Inductor Average Current Mode Control (IACMC) controller in the inner current loop. The IACMC has several advantages, including its robustness when line voltage and output load fluctuate significantly. The PI controller is designed using the BBC's state space average concept. MATLAB/Simulink is used to simulate the proposed system and its control circuit. The simulation findings indicate that a power factor close to unity can be achieved and that there is virtually no change in power factor when a different duty cycle is applied.

**Keywords**— *ac-dc converter, buck-boost converter, inductor average current mode control, pi controller, power factor correction.*

## I. INTRODUCTION

Number of electronic power converters level has arisen substantially in the industrial and domestic area (Chakravarthy & Gudey, 2020). There is a lot of situations where these functions used Alternation Current (AC) to Direct Current (DC) conversion as the conventional method by employing a simple rectifiers of simple diode bridge with a large dc-link condenser. The simple diode bridge rectifiers and generates a lot of harmonic input currents which lead to harmonic distortions as well as low voltage input and perturbations of factor efficient power factor (Santhi & Immanuel, 2018). In decreasing the input current harmonic distortions normally, the power supply will be switched. The three common adjusting power supply topologies that were

employed are buck, boost and buck-boost (Arora, Katiyar & Patel, 2016).

There is a rise of number of high-level power efficacy, energy conservation and more in a lot of devices as it is cost-effective and possess a high-quality solid-state appliance that are easily obtainable (Azazi, Ahmed & Lashine, 2018). Singh, Garg & Bhuvaneswari (2011) stated that mining, electrochemical, AC speed alternating motors, petrochemical and large-scale power supplies are the examples of various industries that employed the power processors. The harmonic current can be pumped into AC which pollutes the powder as these power processors utilize switching machine non-linear existence such as diodes. Active or passive wave forming approaches can be employed in achieving the advancement in power efficiency where active wave formers employed the fast digital processor in observing the alteration of the semiconductor devices which lead to a loss in high switching frequencies. The positive ranking of the wave shaper is also extremely high (Mahmud, Alam & Rahman, 2018). The active filter of the power quality can be enhanced as the harmonics were diminished. This categorizes the non-linear load current and the types of voltage wave as well as standardizing the current input (Saini et al., 2017).

Modi (2017) highlights that deduction of harmonic elements in the current input line were predominantly connected to most of the study of non- linear loads of the power factor correction. The few approaches are accessible in matching the unit power factor or the input unit. Input current distortion can be improved by employing a low-pass filter (LPF) on the input and output despite the fact whether the switches work by employing the external control input. Passive PFC and Active PFC approaches often separated into the Power Factor Correcting (PFC) techniques (Garcia et al., 2013).

By employing the inductor average current mode control, the Power Factor Correction (PFC) for single phase AC-DC Buck-Boost Converter was recommended to be employed in the Continuous Conduction Mode (CCM). A presence of sturdiness as there is a huge line voltage and output load variations is an example of benefit for the peak current and

hysteresis current controllers as The Inductor Average Current Mode Control (IACMC) were employed in standardizing the input current and harmonics at the inner loop (Suresh & Babu, 2016). AC-DC buck-boost is a more cost-effective resolution as it possesses a tinier external element. With a minimal components number, the AC-DC buck- boost can step-up or down the voltages whilst providing a reduced operating duty cycle and a greater efficacy in a broad assortment of input and output voltages. In generating a remarkable output voltage standardization for Buck- Boost Converter (BBC) a PI controller was employed at the outer loop under various terms. Zeigler Nichols are the designer of the settings of the PI controller proportional gain ( $K_p$ ) and integral time ( $T_i$ ) tuning approach as in gaining S – shaped step reaction of BBC curve, the step test was employed. As the frequency line adjust in a big form, in the application IACMC is deemed to be far beneficial that the peak current mode controller. Significant advantages were gained by proposing the approaches compare to the conventional boost converter as it is easily apprehended and employ as well as drawing a sinusoidal input current for any DC voltage situations from AC source (Zaidi & Ali, 2018).

The major drawbacks of the converter systems are they sometimes have a higher reactive power which causes reduces energy efficiency, increases load in the electrical distribution and increases electricity costs. The widespread usage of nonlinear loads in residential, commercial, and industrial buildings has significantly increased the electrical grid's harmonic pollution. Besides, the harmonic material in the electrical system is one of the main challenges in terms of power efficiency. Many AC-DC converters are quoted to have a power factor of better than 0.95 when the true power factor is between 0.5 and 0.75 (Ware, 2016).

Singh, Garg & Bhuvaneswari, 2011 shows a power factor of around 0.80 – 0.87, this power factor is in the safe range, but it is still losing 10% or more than the power factor which can be achieved. While other researchers (Saini et al., 2017) when achieved a higher power factor of 0.99 did it with not for commercial products since those are expensive power factor controller. Most of the simulation-based AC-DC buck boost converter does not include a Graphical user interface to track all the required parameters in one display and can see the changes of one parameter with another. The studies mentioned above shows the loss of power factor for AC-DC converter. This loss contributes to large sum of electricity cost and shorten the lifespan of components.

The power factor is a vital system output parameter and improving the power factor is very important for the system to perform better and more economically. If a system's power factor is low at a given power requirement, then the system that is drawn from the supply needs a considerable Volt-amperes value or a large amount of current. It is also shown that different steps are employed in increasing the power factor of a device. Increasing the quality of energy is an issue that, in recent years, has gained massive attention. PFC is one of the power qualities points that receive greater attention, as demonstrated by the number of producers producing different kinds of integrated power factor correction circuits. Nevertheless, the AC-DC buck-boost converter power factor correction is still seldom used. This project suggests creating the AC-DC Buck-Boost PFC to enhance the near unity power factor.

The main aim of this project is to develop a Buck-Boost converter that improves the input power factor of AC Power Supplies by activating the AC input current waveform.

## II. DESIGN METHODOLOGY

The overall system block diagram is shown in the Fig 1., the block diagram shown consist of the major blocks that were used for developing the system. The sub systems of the major blocks are explained in the section, the blocks which is required for the understanding of the system are explained. The system requires an Ac voltage as an input, the ac voltage is connected to full bridge rectifier block which converts the incoming input Ac voltage to Dc voltage. This converted Dc voltage is passed to MOSFET block which is a n channel, and it acts as a process of providing the duty cycle by acting as a switch. The dc voltage is then passed to inverted buck boost converter block unit where the system consists of an inductor, a diode, and a capacitor. The inverted buck boost converter block is responsible for the buck boost operation of the developed system. The inverted buck boost converter block is connected to the Load, which is a resistive load, this block is connected to the voltage sensor block which consist of a voltage sensor connected to the output of the resistive load. The output of the voltage sensor is connected to the summer which consist of summing function, reference voltage block which is the input for the required voltage is connected to the second port of the summer block. The output of the summer block is connected to the PI controller block, the PI controller block is responsible for equation the variables required for the compensating the output voltage to the reference voltage. The output of the PI and the feedback current from the MOSFET measured using the current sensor block is passed to the summer block. The output of the summer block is passed to the comparator, the comparator block is connected to the gate driver which sends the Pulse width modulation signal to control the output voltage.

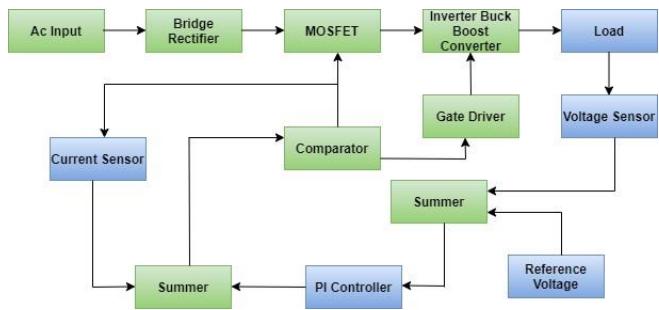


Fig. 1. Block diagram of the proposed system

The connection shown in Fig 2. is the connection of the developed system. The system consists of an 110v 50Hz ac input component, the ac input is connected to the voltage and current sensor and to the input of the full bridge rectifier which is implemented using four diodes in an arrangement by using the bridge circuit configuration which provides the same polarity of output on either polarity of input. The ac component voltage is connected to Total harmonic distortion block and to the power factor calculation block. The output side of the terminal is connected to the drain of the MOSFET, source pin of the MOSFET is connected to the connected to the inductor which is of 70 milli henry and diode. The diode is place is in reverse position hence act as a reverse diode, the diode anode end is connected to the capacitor value of 760 micro farad. The Output is connected to the resistive load of

100ohm, the output of the load is connected to the voltage sensor. The output of the load is connected to the summer positive terminal, the reference voltage is connected to the gain of value -1 then to the negative terminal of the summer block. The output of the summer block is connected to the PI controller, the P and I constant value is provided to the PI controller block. The output of the PI controller is added to the summer block positive terminal, the current output of the inductor is connected to the negative terminal block of the summer. The output of the summer is connected to the relay and the output of the relay is connected to the gate pin of the MOSFET.

The power factor calculation block two inputs are the source current and the source voltage. The source current and voltage are connected to the two different integrator one for each. The output of both the integrator is connected to summer block where the output of the voltage integrator is connected to the positive terminal while the current integrator is connected to the negative terminal. The Output of the summer is connected to gain block, the output of the gain block is connected to the trigonometric Cosine function.

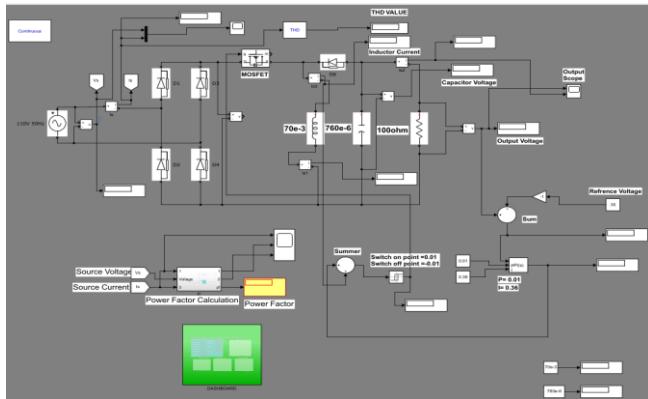


Fig. 2. Connection diagram of the developed system

Fig 3. shows the flow chart of the developed system where the first step is to run the simulation, since the developed system is a buck boost converter the reference voltage is required as an input for the reference voltage. The system checks for the current voltage while the running simulation, this current voltage was then formulated with the reference voltage and the error calculation which can be positive for the buck operation and negative for the boost operation was calculated. The PI controller which is the Outer feedback loop, and which requires the calculated error between the reference voltage and the output voltage as an input. The PI controller output must be tuned for the  $K_p$  and  $T_i$  value for the accurate voltage output, for the tuning method Ziegler Nicholas tuning method was implemented.

For the implementation process the output graph for the signal is then check for the stability, if the graph of the signal was stable enough or less fluctuation for the stability towards the required voltage then the value for the  $T_u$  was calculated. If the graph of the signal was not stable, then the gain value of the differentiator was changed, and the process was implemented until the stable graph was acquired. Also, a step test was performed to obtain the curve of the S form of the step ( $K_p$ ) and integral Time ( $T_i$ ) which was designed using the p response of the buck boost converter. The S shaped curve

of the buck boost converter was characterized by the two parameters delay time and the time constant. The time constant and the delay time were concluded by calculating the tangent line with the line output response. The value of  $K_p$  and  $T_i$  was calculated based on the  $T_u$  value and was set as a constant for the PI Controller. The optimal setting was calculated by calculating the minimum values of the integral of square of error, integral of absolute error and integral of time of square of error. The value of the output is then implemented to the controller which regulates the desired output of the buck boost converter  $K_p$  value was 0.01 and  $T_i$  values was 0.36.

The output of the PI control and of the rectifier output is set to the summer which acts as reference current, the reference current is then compared to the set point voltages and based on the values the PWM pulse is generated which controls the switch of the MOSFET.

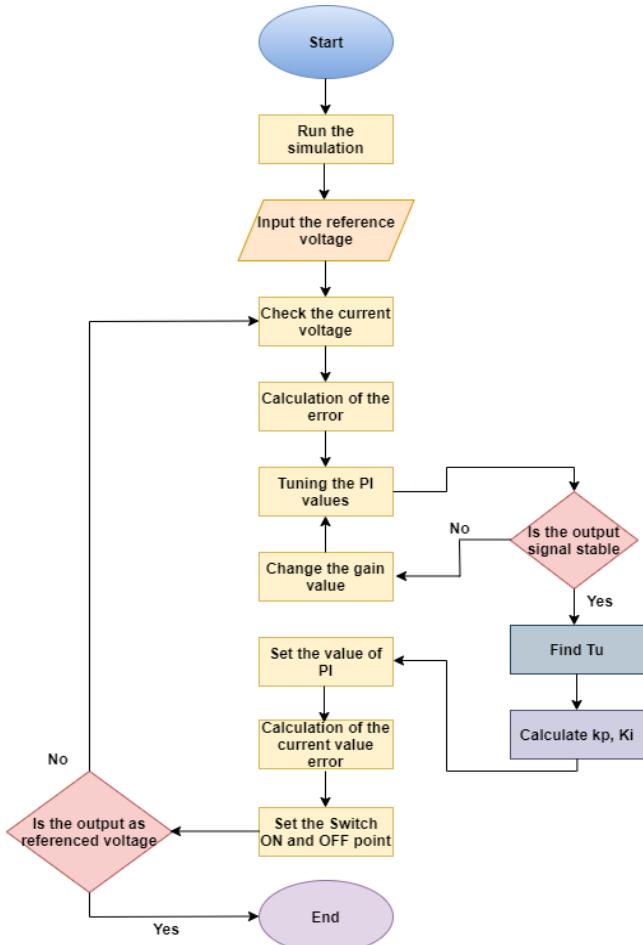


Fig. 3. Flow chart of the developed system

### III. PERFORMANCE TESTING AND SIMULATION RESULTS

The overall performance of the developed system has been evaluated by conducting various simulations using simulation platforms.

#### A. Performance Testing For Buck Boost Operation

This test compares the reference voltage with the output, this test determines the accuracy of the buck boost operation. This test is performed 5 buck and 5 boost operations, the reference voltage and the output voltage are evaluated, and the error percentage was calculated. The setup of this test is done

on the MATLAB/Simulink. The data for buck and boost operation were calculated for 10 instances. The lower side of 30 voltage for buck operation was considered and for 205 voltages for boost operation was considered.

TABLE I. BUCK BOOST OPERATION

Instance	Reference voltage	Output Voltage	Error	Error (%)
1	30	29.9894	0.00035	0.03507
2	50	49.9953	0.000094	0.0094
3	70	70.0212	0.000303	0.0303
4	90	90.0418	0.0004	0.0465
5	105	104.9324	0.00064	0.0643
6	125	125.0167	0.00133	0.01337
7	145	144.9248	0.000518	0.05185
8	175	174.9382	0.00035	0.03526
9	195	194.9317	0.0003501	0.03501
10	205	204.9450	0.00026	0.02678

Fig 4. shows the output voltage with comparison to the reference voltage. The test for the buck operation as well as for the boost operation shows a very marginal error, all the operation was less than 0.1% error where the maximum error percentage was 0.0643 when the reference voltage was 105v, but the output voltage was 104.9324v. The lowest error percentage was 0.0094 %, when the reference voltage was 50v, but the output voltage was 49.9953v. The maximum and minimum error % was lower than 0.1% which can easily be neglected, and the fluctuation can be due to the PI voltage loop controller which is not completely stable.

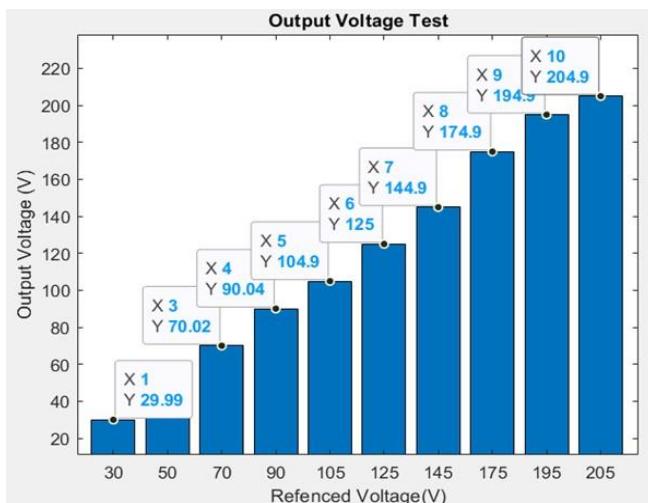


Fig. 4. Output voltage test

#### B. Performance Analysis of Proposed And Conventional Buck-Boost Converter for Power Factor

This test compares the power factor analysis of the developed buck-boost converter for several different duty cycle. This test is performed for 9 different duty cycle and the power factor were calculated and noted. The setup of this test is done on the MATLAB/Simulink. The data for buck and boost operation were calculated for several instances. The

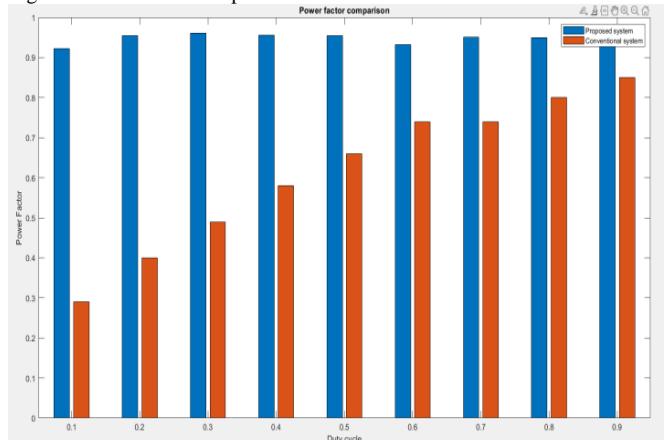
lower side of duty cycle is 0.1 and the higher side of the duty cycle is 0.9. The collected data were noted down and analysis is done further.

TABLE II. POWER FACTOR

Instances	Duty Cycle	Power Factor	
		Conventional AC-DC Buck Boost Converter	Proposed AC-DC Buck Boost Converter
1	0.1	0.29	0.9223
2	0.2	0.40	0.9552
3	0.3	0.49	0.9612
4	0.4	0.58	0.9553
5	0.5	0.66	0.9551
6	0.6	0.74	0.9324
7	0.7	0.74	0.9513
8	0.8	0.80	0.9491
9	0.9	0.85	0.9321

Fig 5. shows the power factor contrast between the proposed buck boost converter versus the conventional buck boost converter. The power factor comparison shows a visible significant improvement of the proposed buck boost converter. The lowest power factor value of the conventional buck boost converter was 0.29 when the duty cycle was at 0.1(lowest) and the highest power factor was 0.85 when the duty cycle was 0.9. for the proposed buck boost converter, the lowest power factor was 0.9223 when the duty cycle was 0.1 and the highest was at duty cycle of 0.3 where the value of the power factor was 0.9612. There is a drastic improvement of 8% between the lowest power factor of the analyzed system where the proposed system is showing a vastly improved system. Though it has been found that the power factor is lowest and lower at the highest and lowest end of the duty cycle. The non-ideal characteristic of the MOSFET switch is the reason behind it.

Fig. 5. Power factor comparison



#### C. Performance Analysis of Total Harmonic Distortion for Proposed and Conventional Buck Boost Converter

This test is for the calculation of the total harmonic distortion for different duty cycle and compares the result between both buck boost converter. This test is performed for 9 different duty cycle and the Total harmonic distortion were

calculated and noted. The setup of this test is done on the MATLAB/Simulink. The data for buck and boost operation were calculated for 10 instances. The lower side of duty cycle is 0.1 and the higher side of the duty cycle is 0.9. The collected data were noted down and analyzation is done further.

TABLE III. HARMONICS DISTORTION ANALYSIS

Instances	Duty Cycle	Total Harmonics Distortion	
		Conventional AC-DC Buck Boost Converter	Proposed AC-DC Buck Boost Converter
1	0.1	0.29	0.89
2	0.2	2.20	1.19
3	0.3	1.70	0.72
4	0.4	1.38	1.12
5	0.5	1.11	0.92
6	0.6	1.89	0.97
7	0.7	1.72	1.24
8	0.8	1.70	0.93
9	0.9	1.61	0.97

Fig 6. shows the comparison of the Total harmonic distortion between the proposed buck boost converter versus the conventional buck boost converter. The data shows an improvement of the Total harmonic distortion of the proposed system over the conventional AC-DC buck boost converter. The highest THD of the conventional AC-DC buck boost converter is 2.20 while for the proposed buck boost converter is 1.24. If we take the average THD of the conventional buck boost converter is 1.511 while for the proposed system, the average THD is 0.994.

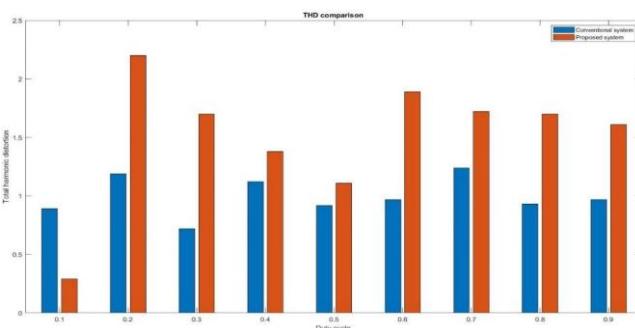


Fig. 6. THD comparison

#### D. Performance Testing Under Varying Load

This test is for the analysis of the performance of different values of resistive load. This test is performed for 10 different values of the resistive Load and check the power factor and output voltage. The reference voltage is set for 150volts. The data for buck and boost operation were calculated for 10 instances. The lower value of resistive load is  $110\Omega$  and the higher value of the resistive load is  $200\Omega$ . The collected data were noted down and analyzation is done further.

TABLE IV. UNDER VARYING LOADS

Instance	Resistive load (ohm)	Output Voltage (Volts)	PF	THD
1	110	150.51	0.9722	0.93
2	120	150.73	0.9684	0.92
3	130	149.52	0.9642	0.95
4	140	150.89	0.9596	0.92
5	150	148.92	0.9510	1.14
6	160	149.36	0.9421	1.21
7	170	149.53	0.9373	1.46
8	180	150.87	0.9324	1.18
9	190	151.22	0.9310	1.89
10	200	149.34	0.9285	1.63

Fig 7. shows the comparison of the output parameters with respect to change in Load. As compared to referenced voltage the maximum change occurred when the resistive load was set to 180 and the output voltage was 151.22v which shows a deflection of 1.22v. The lowest deflection was at when the resistive change was very less at  $110\Omega$  the output voltage was 150.51v which shows a change of 0.49 volts. The power factor clearly changes with the change in resistive load, the best power factor occurred at the lowest change in load  $110\Omega$  where the value was 0.9722 while the highest loss in power factor was at load  $200\Omega$  at which the power factor value was 0.9285. The change in the power factor can be justified since the change in load cause the change in power factor angle with the load, the results cause lesser leading angle and hence more lagging nature which decreases the power factor value. And since the relationship between power factor and THD states that the lower the THD in power system the higher the power factor. Hence when the power factor was decreasing so the THD was increasing.

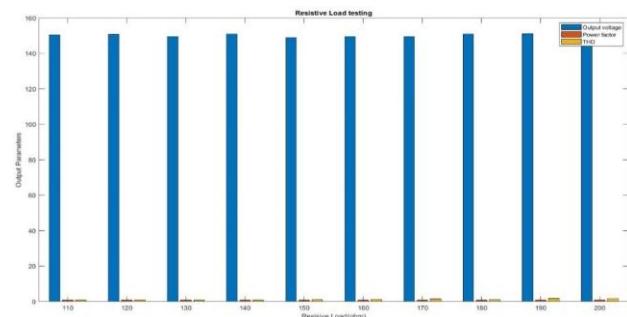


Fig. 7. Resistive load test

#### E. Performance Analysis of Proposed And Conventional Buck-Boost Converter for Efficiency

This test compares the efficiency analysis of the developed buck-boost converter for several different duty cycle. This test is performed for 9 different duty cycle and the efficiency werecalculated and noted. The setup of this test is done on the MATLAB/Simulink. The data for buck and boost operation were calculated for severalinstances. The lower side of duty cycle is 0.1 and the higher side of the duty cycle is 0.9. The collected data were noted down and analyzation is done further.

TABLE V. EFFICIENCY PERFORMANCE ANALYSIS

Instances	Duty Cycle	Conventional AC-DC converter	Proposed AC-DC converter
		Efficiency (%)	Efficiency (%)
1	0.1	80.51	93.42
2	0.2	91.11	98.10
3	0.3	95.19	99.46
4	0.4	97.28	99.33
5	0.5	98.41	99.18
6	0.6	98.95	98.27
7	0.7	99.01	95.42
8	0.8	98.78	94.10
9	0.9	96.93	97.14

Fig 8. shows the efficiency comparison between the proposed buck boost converter with the conventional buck boost converter. For the conventional buck boost converter, the lowest efficiency was 80.51% when the duty cycle was at 0.1 and the highest was 99.01 at duty cycle of 0.7. The proposed buck boost converter the lowest efficiency was 93.42% when the duty cycle was at 0.1 and the highest was 99.46% at duty cycle of 0.3. The average efficiency of the conventional buck boost converter is 95.13% while the proposed buck boost converter efficiency is 97.16%. This shows the performance of the proposed buck boost converter is more efficient than the conventional buck boost converter. The conventional buck boost converter produces a higher ripple voltage and current as compared to proposed system, since the proposed system uses a two-loop controller to reduce ripple current and ripple voltage.

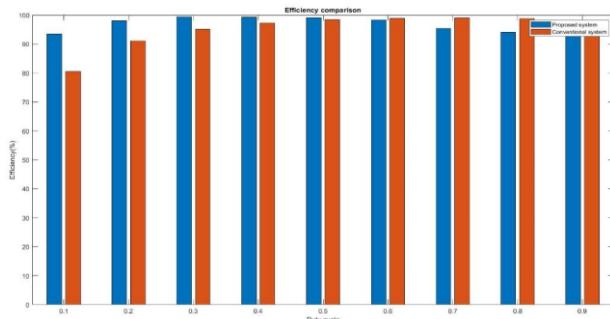


Fig. 8. Efficiency comparison

#### IV. CONCLUSION

The proper AC to DC buck boost converter system has been successfully designed which has a higher power factor and lower total harmonic distortion. The outer loop implementation of the PI controller is at its peak of performance, which helps in output voltage regulation for BBC under a wide range of conditions. The PI controller design incorporates the Ziegler Nicholas method for tuning, and the inclusion of ICAMC is advantageous compared to peak current mode controller in applications where the line frequency is changing slowly. According to the simulation results, it seems as though there will be nearly a constant

power factor when the line frequency is at various ranges, which agrees with the experimental results. The results shows that the lowest power factor value of the conventional buck boost converter was 0.29 when the duty cycle was at 0.1(lowest) and the highest power factor was 0.85 when the duty cycle was 0.9. for the proposed buck boost converter, the lowest power factor was 0.9223 when the duty cycle was 0.1 and the highest was at duty cycle of 0.3 where the value of the power factor was 0.9612. The highest THD of the conventional AC-DC buck boost converter is 2.20 while for the proposed buck boost converter is 1.24. If we take the average THD of the conventional buck boost converter is 1.511 while for the proposed system, the average THD is 0.96.

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