Gate Driver for SiC MOSFET

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Abstract*— SIC Mosfet plays a huge role in power converters and it works under high voltage, high switching frequencies and high temperatures. SiC MOSFETS are widely used in converters are inverters due to their strength but, when connected in half-bridge configurations, there are positive and negative voltage spikes when switching at high frequencies which triggers the lower Mosfet to turn ON and threatens the safe operation of the device. This project focuses on minimizing the voltage spikes by using two capacitors in parallel with resistors which will be able to generate negative voltage without the need of an external power source. This negative voltage will shift the positive and negative voltage spikes below the threshold voltage of the SiC MOSFET so that the device could operate safely. After performing simulation testing using LTspice, it was seen that even at the frequency of 1MHz the gate driver was able keep the voltage spike below the threshold voltage of the SiC MOSFET. The maximum voltage spike was recorded to be 1.3V at 1MHz and 0.08V at 100KHz. As for future recommendations for the enhancement of this project, a much fast switching PNP transistor could enhance the results and if the gate driver is to be used roughly around 100KHz, a diode can be added along the base and emitter of the PNP transistor which would help to create a low impedance path to the negative voltage generated by the capacitors.

***Keywords*— Gate Driver for SiC MOSFET, Voltage spikes**

I. INTRODUCTION

In modern world the use of electricity is the very essence of life and with the use of electricity, efficient devices are made to help mankind. These devices contain electronic parts which are responsible for the functions that are carried out by devices such as mobile phones, computers, electronic cars, satellites etc. Almost all the electronics makes the use of transistor which is a crucial part of power electronics. Transistors are widely used in power converters/inverters, amplifying circuits, voltage and current controllers etc [1]. The old Si based transistors were the most crucial component in the power electronics but, with the technological advancements a more efficient transistor was required. Modifications were made to the Si based transistors which would help it to work under higher power density and higher switching frequencies. There was need for a new type of transistor which could operate safely under high pressure with a simpler circuit. The invention was made by using SiC and GaN in transistors which were more efficient compared to Si transistors and could work under high power density and high switching [2].

In comparison with the Si based transistors, SiC transistors could operate at much high switching frequency, higher power density, higher operateable temperatures and much lower losses than the Si based transistors. However, with the increase of the switching speed there are losses which induces oscillations, overshoots, negative current, electromagnetic interference and additional losses. The purpose of the project will be to modify the gate driver of the MOSFET in such a way that these losses could be minimized and to make the MOSFET more efficient. the new SiC MOSFETS are used commonly in power converters and inverters which would be focus of this project.

The main issues faced by the SiC mosfet are the switching losses, overshoot of current and voltage, induced EMI and stray inductances when operating at a higher switching speed. In the study carried out by the researcher [1] it can be seen that SiC MOSFETs have a higher ON state resistance when compared to Si based transistors, so in order to keep the voltage at a certain level the gate driver voltage would need to be higher, also a lower ON state resistance will help in reducing the conduction losses. The gate drivers for the Si transistors cannot be used for the SiC MOSFET as they have a lower operating voltage (10V-15V). SiC MOSFET need to operate at high voltages because the higher the voltage the lower will be there ON-state resistance which is why different gate drivers are required for SiC transistors. [3]

This research focuses on the voltage spikes which occur in half-bridge and full-bridge power converters. These voltage spike need to be minimized because these voltages can trigger an un wanted turn ON of SiC MOSFET. These voltages occur when the upper MOSFET is supplied the voltage, the stray capacitance at gate source terminal charges up due to which a voltage spike occurs in the lower MOSFET and these voltage spikes can trigger the lower MOSFET to turn ON. To avoid this unwanted turn ON of the SiC mosfet, a gate driver is designed which can provide a negative voltage to the voltage spikes which would help in minimizing the voltage spikes and minimizing the chances for the unwanted turn ON [4]. Therefore, the aim of this research is to design a gate driver for SiC MOSFET which will help in minimizing the voltages spikes occurred during high switching frequencies.

[5] focused on gate drivers designing and the key factors that can help in producing a high efficiency gate driver for SiC mosfets. There are already some manufactured mosfets available in the market with high frequency and efficiency which are replacing the previous IGBT transistors rapidly. The researcher states that to gain full advantage over the SiC Mosfets, a new breed for gate drivers is needed. Parasitic inductances and capacitances play a major role in the gate drivers performance while operating at high frequencies so ideally the gate driver should be placed very near to the SiC mosfet and the parasitic elements can be minimized. [3]

presented several gate drivers topologies available for SiC mosfet and compared them in term of efficiency, complexity and cost with some comparison between SiC transistors and Si transistors. The author discussed the resonant gate drive circuit. The principle on which the circuit is based upon is that an inductor is connected to gate of mosfet in series which when releases energy stored in it to the gate and due to the high current the mosfet turns ON very fast. As the turn ON time is shortened the switching will be fast and thus there are less losses. [1] discussed about the properties of SiC mosfets including some of their advantages over the previous Si based transistors. Furthermore, the researcher discussed about the uses of SiC mosfet and the challenges that need to be solved and had presented some of the gate driver topologies that would be suitable for the mosfet by comparing their results. Some of the advantages that SiC mosfet has over Si based transistors is that SiC mosfet can withstand high DC link voltage, operate at high temperatures (150°C-175°C) and can function at higher switching frequencies. As the device operates at higher switching speeds the device in more likely to have EMI issues and it affects the overall performance of the device. SiC mosfet have an issue of negative voltage spike which can turn ON the device accidently.

The high-speed switching of SiC MOSFET leads to a side effect of increasing electromagnetic interface (EMI). Hence, the early studies in SiC MOSFET gate driver mainly focused on these EMI effects [6-9]. [2] proposed a new topology for SiC mosfet gate drivers. This gate driver as named by the researcher as Active Gate Driver or AGD had reduced the over-shoot of voltage and noise and also kept the switching losses to a minimum. The operating principle of this gate driver is to have two different resistive paths during the switching phase. The flow of the current is controlled by two different switches and each of the switches are connected to a voltage comparison range which is the voltage of gate source terminal right before and during the miller plateau range. [4] proposed a gate driver which minimizes the positive and negative voltage spikes occurred during the turn on and turn off of the phase-leg configured buck converter. These positive and negative voltage spikes are responsible for the unwanted turn ON of the transistor. According to the researcher, the first function of the gate driver is to reduce the positive voltage spike by generating a negative gate voltage which also helps in reducing the turn off time. The gate driver uses two resistors to create a voltage divider which can generate different negative gate-source voltages depending on their values without the need of an external voltage source. [10] focuses on minimizing the spurious turn on in bridge-leg configured MOSFET. There are two ways in which this issue was dealt previously, the first was to reduce the switching speed so decrease the magnitude of spurious triggering pulse and the second was to minimize the impedance at the gate path of transistor. By slowing down he switching speed, there was an increase in switching losses.

[11] presented two equivalent circuits to test out the switching oscillation phenomenon of SiC mosfet and had presented simple formulas to explain the and guide the snubber circuit design. The researcher presented an equivalent circuit with RLC circuitry and an inductive load circuit and compared them to better understand the ringing effect in the SiC mosfet. At the very first sight it was noticed by the researcher that the inductive load circuit had some delay to its oscillations as compared to the RLC circuit because it takes a few moments for inductive load circuit to charge up the mosfet, so if the mosfet can be turned ON faster the oscillations can be reduced and matched with the RLC circuit. [12] proposed an Active Gate Driver which was used to overcome the issue of oscillations which occurred in the SiC mosfet due to high switching frequency. The proposed gate driver focuses on reducing these losses in the turn OFF phase. The proposed gate driver was able detect the rise drain source voltage and it could generate positive pulse in the drain current during its current fall which resulted in the gate voltage increment and results in reducing the drain voltage spikes and oscillation. The researcher proved that to overcome voltage spikes and oscillations, the voltage for the gate source terminal must be kept higher.

[13] proposed a gate assisted circuit (GAC) which is then connected to a PMOS transistor and a capacitor. The testing circuit design is configured to be half-bridge circuit using SiC MOSFETs. The PMOS transistor and the capacitor and connected in series with each other and they both are then connected to gate-source of the SiC MOSFET in parallel. The main purpose of PMOS is to prevent the shoot through voltage during the turn on and turn off phase. The operation of the gate driver is divided into four intervals, in the first interval the lower MOSFET is turned on and the upper is turned off and the upper capacitor starts to charge. In the second interval the switches are kept the same but the negative voltage supply starts which charges the upper MOSFET's Cgs. [14] proposed a gate driver which can help the SiC mosfet to switch at high frequency with low losses and low noise. The proposed gate driver is a boost circuit with reduced the losses and the delay time and it kept the switching noise from increasing. According to the researcher, the switching losses and noise mainly have a tradeoff between them and it is hard to lower one of them without increasing the other, but the researcher managed to design a gate driver to have low losses and while maintain the noise at a certain level. This circuit enables the SiC mosfet to turn ON rapidly and also uses a discharge capacitor which helps to reduce the turn OFF timing. This gate driver has included two diodes which help to change the flow of current during the switching process.

II. PROPOSED SYSTEM METHODOLOGY

Fig. 1 shows the block diagram of the half bridge configuration of a converter in which uses SiC MOSFET. The SiC MOSFET's gate terminal is connected to the gate driver. The PWM signal provides the input voltage to the gate driver and the SiC MOSFET. The main purpose of the gate voltage is to provide a negative voltage which will then reduce the voltage spikes occurred during the fast switching. The gate driver reduces the voltage spikes just below the threshold voltage of the SiC MOSFET (2.8V) and thus reducing the unwanted turn ON of the MOSFET.

Fig. 2 represents the gate driver circuit and shows the connections for the entire system.. The capacitor C1 connected in parallel with resistor R1 helps in preventing the shoot through voltage by generating a negative voltage which reduces the shoot through voltage and prevent the unwanted turn ON. The resistor R2 is connected to the PNP transistor and helps in turning ON the PNP transistor. When the voltage drop on R2 would be large enough the PNP transistor will turn on and connect the capacitor C2 to the circuit which will boost the charging of the gate-source capacitance Cgs thus reducing turn ON time. A small gate resistance Rg is used because the

smaller the gate resistance the larger voltage drop will be on R2 and thus the PNP transistor can remain ON for longer.

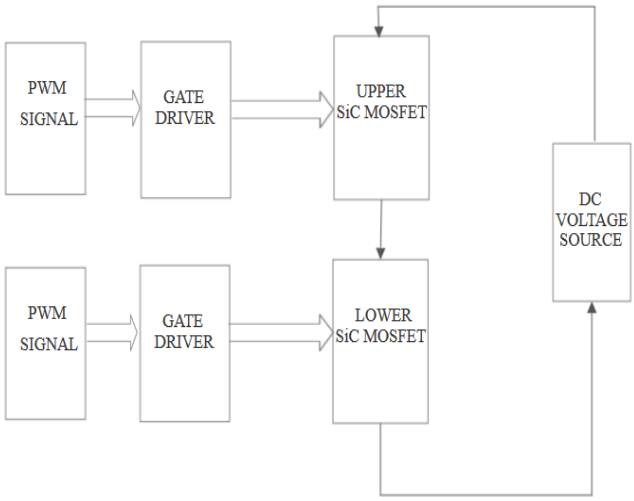

Fig. 1. Overall block diagram of the entire system

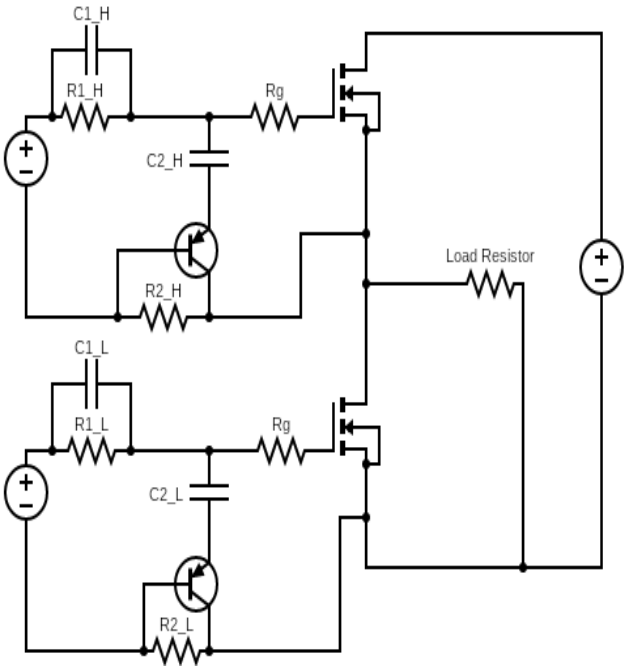

Fig. 2. Wiring diagram of the gate driver

The basic working principle of the system is voltage level shifter. The main idea of the voltage level shifter is to reduce the voltage spikes below the threshold voltage of the SiC MOSFET so that the unwanted turn ON of the MOSFET can be prevented. This is achieved by connecting two capacitors in parallel to each other which can generate negative voltages. The capacitor C1 is connected in parallel with a resistor to control the charging of the capacitor and thus the negative voltage generated can be controlled by changing the value of the resistor. A small gate resistance is added to the circuit which helps in keeping the PNP transistor remain in ON state for a longer time period thus the capacitor C2 can help in reducing the voltage spike. During the turn ON of the upper MOSFET, the voltage drop on R3 would be higher transistor will turn ON connecting C2 to the circuit. Capacitor C2 will boost the charging of Cgs of the upper MOSFET thus reducing the turn ON time of the MOSFET. Part of current will flow towards the lower MOSFET and charge the capacitor Cgs of the lower MOSFET and increase the gate voltage of the MOSFET which can trigger it to turn ON. The gate driver added to the lower MOSFET will provide the negative voltage through C1 and thus minimizing the voltage spike and preventing the turn ON of the device.

During the turn OFF of the upper MOSFET, the capacitor C1 provides a negative voltage to the gate source capacitance Cgs of the upper MOSFET through R3 and helps in discharging of Cgs. The voltage drop on R3 will make the voltage Part of the inductive current through upper MOSFET will shoot through to lower MOSFET and charge Cgs of lower MOSFET. C1 of the lower MOSFET will provide a negative voltage to suppress the voltage spike but gradually the voltage drop at R3 will increase due to the stray inductances, the PNP transistor will turn ON and connect C2 to the circuit. This will provide a low impedance path thus a large amount of this current flows through C2 to the capacitance Cdg of the lower MOSFET and thus Cdg will release its energy and suppress the voltage spike. A brief description of the working principle is given in the flowchart shown in Fig. 3.

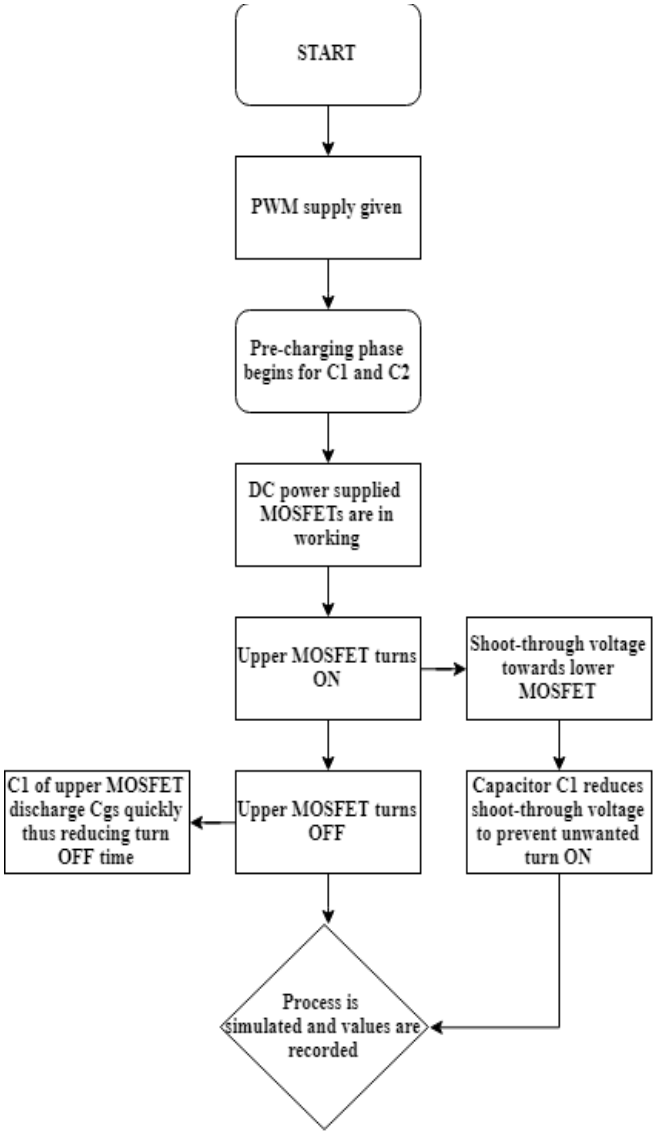

Fig. 3. Flowchart representation

III. SIMULATION RESULTS

The working principle and the operation of the gate driver has been explained in the previous sections. The gate driver designed needs to be simulated to understand its voltage suppression capability. The software used for the simulation of the gate driver is LTspice. Following are some of the results obtained from the simulation such as negative voltage spike and switching speed. The parameters for the simulation are listed in Table I. Fig. 4 shows the positive and negative voltage spikes occurred in the lower MOSFET during switching, Figures 4 and 5 shows the turning ON speed of the lower MOSFET and Fig. 6 shows the turning OFF speed of the lower MOSFET for the given parameters.

TABLE I. SIMULATION PARAMETERS

R1	*R2*	*Rg*	*C1*	*C2*	*Input pulse Voltage*	*Frequency*	*Vdc*
2.5kΩ	2Ω	5Ω	0.2 µF	0.1 µF	0V-24V	100KHz	400V

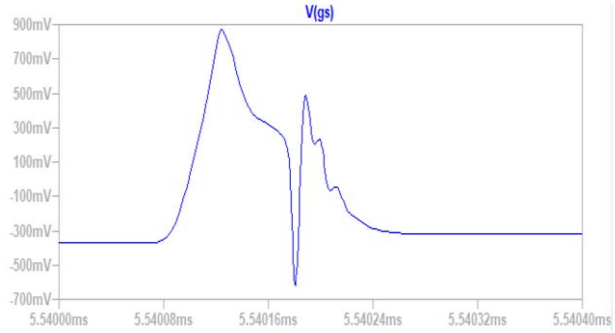

Fig. 4. Positive voltage spike in lower MOSFET

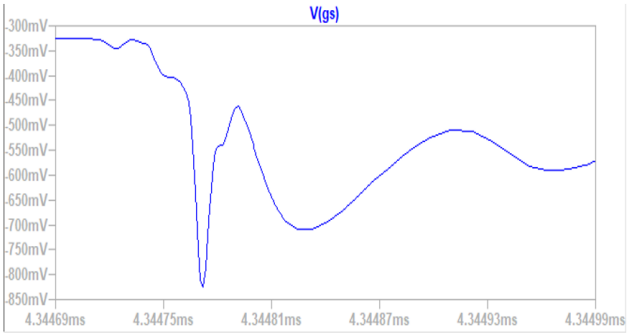

Fig. 5. Negative voltage spike in lower MOSFET

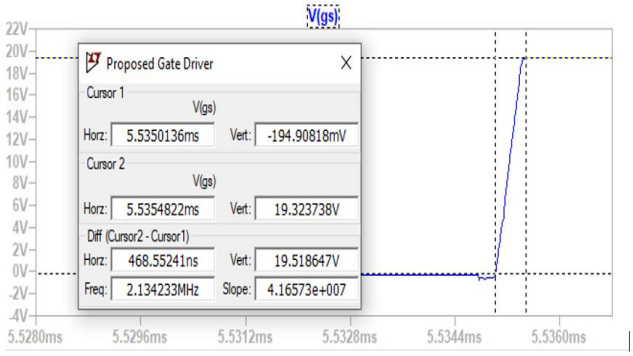

Fig. 6. Turn on of lower MOSFET

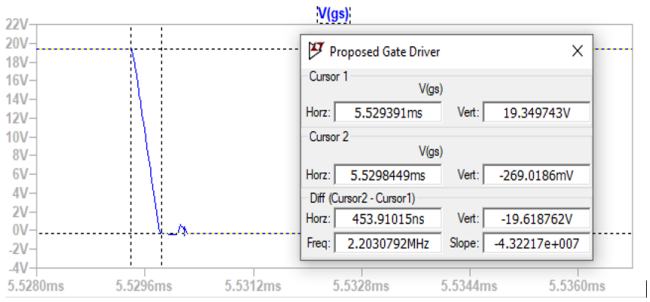

Fig. 7. Turn off of lower MOSFET

Table II. displays the values obtained from these figures. The positive voltage spike occurs during the turning ON of the upper MOSFET and the positive voltage spike is noted to be 0.822V. The main purpose of the gate driver was to shift the voltage spike lower than the threshold voltage of the SiC MOSFET which is 0.28V according to the datasheet. The negative voltage spike is noted to be -0.821V which occurs during the turn OFF of the upper MOSFET. The switching speed are displayed in Figures 5 and 6 from which we can the turning on speed is 468.55ns and turning OFF speed is 453.9ns. These values obtained are for the parameters shown in Table I. Further testing will be done in the next chapter which will show the voltage spikes and switching speeds for different frequencies, input voltages and comparison with a conventional gate driver and comparison from a gate driver explained in literature review.

TABLE II. VALUES OBTAINED FROM SIMULATION

Positive voltage spike	*Negative Voltage spike*	*Turning ON speed*	*Turning OFF speed*
0.822 V	-0.821 V	468.55 ns	453.9ns

IV. TESTING AND FINDINGS

A. *LOWER MOSFET VOLTAGE SPIKES TEST*

For this experiment the positive and negative voltage spikes will be compared for different frequencies to illustrate how the gate driver operates at different frequencies. Three frequencies are selected which are 10KHz, 100KHz and 1MHz on which the Vgs of lower MOSFET will be tested on. The dotted line represents negative voltage spikes and a normal line is used to represent the positive voltage spikes in Fig. 8 According to the working principle of the gate driver, the voltage spike will be shifted below the threshold voltage of the SiC MOSFET so that the unwanted turn ON of the device can be prevented. The threshold voltage of the SiC MOSFET model C2M0040120D is 2.8V according to its data sheet. The positive voltage spike of the proposed gate driver is lower than the threshold voltage for all the selected frequencies i.e. low frequency, normal frequency and high frequency as shown in Fig. 8. Also it can be seen that as the frequency is higher the voltage spikes increases which can be due to the improper charging and discharging of the capacitors. The other factor that effects the voltage spikes at higher frequencies is the switching speed of the PNP transistor which can be solved by reducing the frequency or by selecting a different model transistor. However, the best working frequency for the gate driver and the SiC MOSFET is 100KHz-500KHz under which the overall performance of the device is efficient including the suppression of voltage spikes.

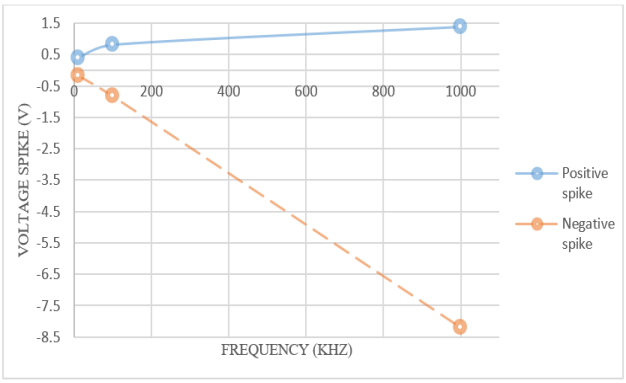

Fig. 8. Lower MOSFET's voltage spike graph

B. *Upper MOSFET voltage spikes Test*

For this experiment the positive and negative voltage spikes will be compared for different frequencies to illustrate how the gate driver operates at different frequencies. Three frequencies are selected which are 10KHz, 100KHz and 1MHz on which the Vgs of upper MOSFET will be tested on. Table III. displays the results obtained for Vgs with the given frequencies.

TABLE III. VOLTAGE SPIKES FOR UPPER MOSFET

Frequencies	***Positive Voltage spike***	***Negative Voltage spike***
10KHz	0V	0V
100KHz	-0.140V	-0.219V
1MHz	-2.976V	-9.325V

The dotted line represents negative voltage spikes and a normal line is used to represent the positive voltage spikes in Fig 9. The positive and negative voltage spikes for the upper MOSFET are considerably lower than that of the lower MOSFET because the switching of the upper MOSFET results in voltage shoot through to the lower MOSFET but the switching of the lower MOSFET has little to none effect on the upper MOSFET. At the normal frequency (100KHz) the positive and negative voltage spikes are normal and the positive voltage spike is lower than the threshold voltage. At lower frequency (10KHz) the voltage spike is very low so it is considered to be 0V.

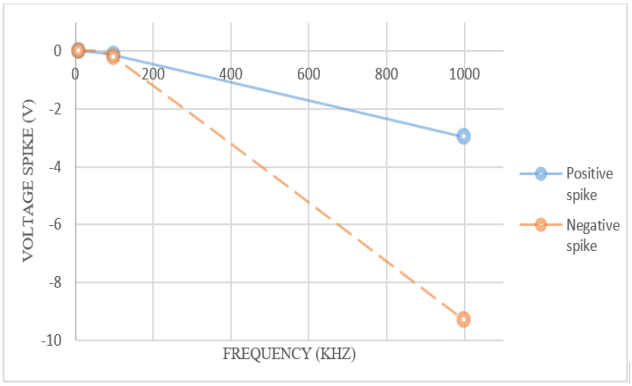

Fig. 9. Upper MOSFET's voltage spike graph

C. *Lower MOSFET switching speed*

For this experiment the turn ON and turn OFF switching speed of the lower MOSFET will be tested and compared at different frequencies to illustrate how the gate drive effects the switching speeds at different frequencies. Three frequencies are selected which are 10KHz, 100KHz and 1MHz on which the switching speed of the lower MOSFET will be tested on. Table IV. displays the results obtained for turn ON and turn OFF switching speed with the given frequencies.

TABLE IV. SWITCHING SPEED FOR LOWER MOSFET

Frequencies	***Turn ON***	***Turn OFF***
10KHz	3993.34ns	4103.16ns
100KHz	441.26ns	447.73ns
1MHz	47.92ns	88.44ns

The dotted line represents turn OFF speed and a normal line is used to represent the turn ON speed in Fig. 10. For higher frequency of 1MHz the switching speed is quite fast because of the input but there is a big difference between the turning ON and turning OFF speed which is mainly because of the recovery of the MOSFET and the discharging of its Cgs. The turning OFF speed is still better which will be explained clearly while comparing the gate driver with other gate driver design and a conventional gate driver. The difference between the turning ON and turning OFF speed is better for normal frequency as it only has a difference of 6.47ns which is due to the reason that the SiC MOSFET recovery and discharging is better at this frequency range.

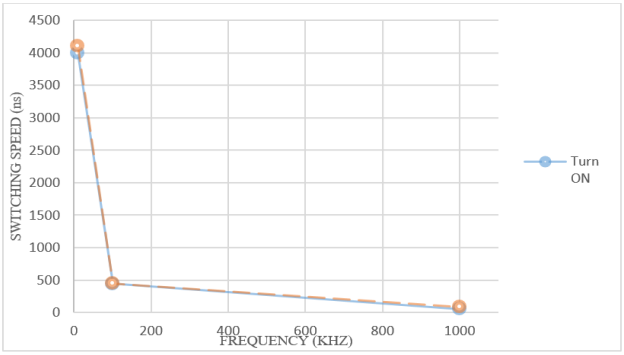

Fig. 10. Lower MOSFET's switching speed graph

D. *Lower MOSFET oscillation*

For this experiment the oscillation for the lower MOSFET will be tested and compared at different frequencies to illustrate how the gate drive effects the oscillation at different frequencies. Three frequencies are selected which are 10KHz, 100KHz and 1MHz on which the oscillation of the lower MOSFET will be tested on. Table V. displays the results obtained for oscillation with the given frequencies.

TABLE V. OSCILLATION FOR LOWER MOSFET

Frequencies	***Peak to peak Voltage***	***Time***
10KHz	0V	0ns
100KHz	1.617V	76.77ns
1MHz	10.4V	95.81ns

From Fig. 11 as the frequency increases the oscillation also increases due to the high voltage spikes but at normal or lower frequencies the oscillation is very little to none. Also from Fig. 12, we can see that at higher frequency the oscillation takes more time to settle down as the oscillation is high so it does require some time to reach steady state. For normal frequency the time it takes for the oscillation to reach steady is low and

as for low frequency there is no oscillation so the time is also zero.

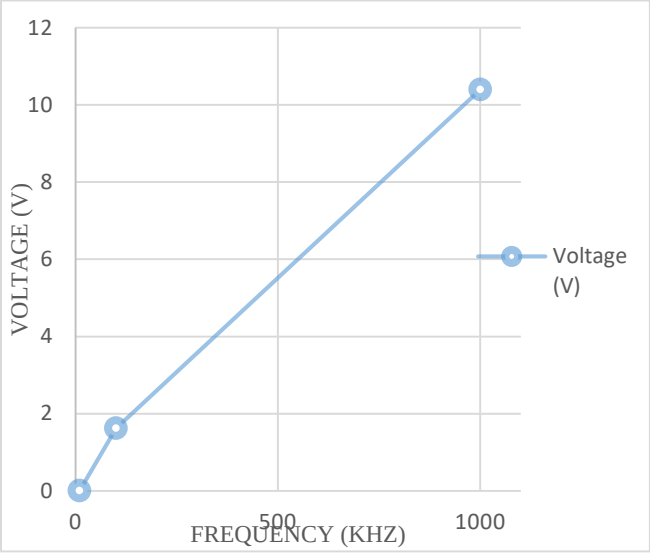

Fig. 11. Lower MOSFET peak-peak voltage oscillation graph

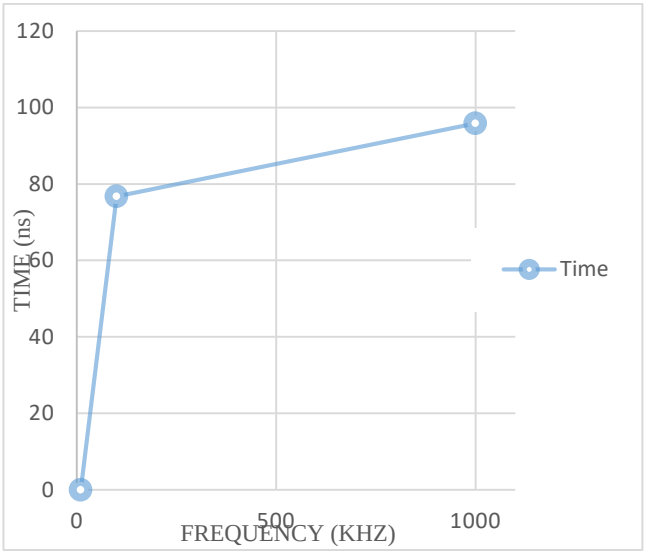

Fig. 12. Lower MOSFET oscillation time

V. DISCUSSION

after performing different tests it can be seen that the voltage spikes had been suppressed. Even at very high frequency the positive voltage spike is still lower than the threshold of the SiC MOSFET. So it can be concluded that the first objective has been successfully achieved. Different testing was done on the proposed gate driver such as voltage spikes for lower and upper MOSFET were tested, switching speed of the lower MOSFET was tested and the voltage drop at load and its switching speed was tested. All the tests were performed for different frequencies ranging from low to high frequencies. From these tests we can conclude that the overall performance of the gate driver was significantly good as it was able to prevent the unwanted turn ON of the device by reducing the voltage spike and the second objective has been successfully achieved. The proposed gate driver was far better than the conventional gate driver as it had lower positive voltage spikes than the conventional gate driver at low and high frequencies. The proposed gate driver was able to prevent the unwanted turn ON of the device but the conventional gate driver had much larger voltage spikes and was not able to prevent the unwanted turn ON. The gate driver from literature review and the proposed gate driver were both able to prevent the unwanted turn ON of the device at low and high frequencies and the switching speed of the device was also similar.

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